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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Edward A. Burton et al.

Title: APPARATUS AND METHOD TO CONTROL SELF-TIMED AND SYNCHRONOUS SYSTEMS

Docket No.: 884.C02US1
Filed: December 31, 2003
Examiner: Anh-Quan Tra

Serial No.: 10/750,320
Due Date: August 16, 2006
Group Art Unit: 2816

MS Appeal Brief - Patents
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REPLY BRIEF UNDER 37 C.F.R. § 41.41

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APPELLANTS' REPLY BRIEF

This Reply Brief is filed in response to the Examiner's Answer (hereinafter, the "Answer"), mailed June 16, 2006, and supplements the Appeal Brief filed by the Appellants on April 3, 2006. Please charge any required additional fees or credit overpayments to Deposit Account 19-0743.

Argument

Appellants submit that the Final Office Action, even when considered in view of the additional comments provided in the Answer, fails to meet the burden of setting forth a *prima facie* case of anticipation and a *prima facie* case of obviousness in rejecting claims 1-20 and 26-30.[1]

The Final Office Action fails to set forth a prima facie case of anticipation in rejecting claims 1-2, 6-18, 26-27, and 29 in view of Mizuno et al. because the Office Action fails to show how Mizuno et al. discloses all of the subject matter included in each of claims 1-2, 6-18, 26-27, and 29.

1 The Appellants have reviewed the Answer, and believes the statements in the original Appeal Brief remain accurate and compelling. In reply to the Answer, the Appellants wish to further clarify certain points of distinction between the pending claims and the cited documents in response to newly presented comments. The corresponding pages of the Answer will be used to reference each of these points.

In addition, Appellants maintain each and every argument submitted in Appellants' pending Appeal Brief, and respectfully submit that each of the arguments are proper and valid in view of all of the statements made in the Answer. Therefore, any lack of reference in this Reply Brief to a particular argument in the pending Appeal Brief is not to be construed as an admission that the Appellants agree with any of the statements in the Answer. Appellants ask that the statements made in Appellants' pending Appeal Brief be considered in full, in addition to the statements included with this Reply Brief.

Appellants maintain, as argued on pages 10-12 of the Appeal Brief, that the Final Office Action fails to set forth a *prima facie* case of anticipation in the rejection of 1-2, 6-18, 26-27, and 29 because the Final Office Action (and now the Answer) have not shown that Mizuno et al. discloses the identical invention as claimed in claims 1-2, 6-18, 26-27, and 29, and so these claims are not anticipated by Mizuno et al.

Using claim 1 as an example, claim 1 recites, "a **leakage timing circuit** formed on the substrate, the **leakage timing circuit** having a frequency related to **a leakage current**." (Emphasis added). Thus, claim 1 refers to a leakage timing circuit (*not* an individual device such as a single transistor) having a frequency related to a leakage current. FIG. 4B and FIG. 4C in Appellants specification illustrate embodiments of leakage timing circuits, which are described in Appellants specification on page 11, line 14 through page 12, line 16.

In contrast, the Final Office Action and the Answer contend that OSC20 in FIG. 12 of Mizuno et al. discloses the above quoted subject matter from claim 1. In the Final Office Action and in the Answer, OSC20 is incorrectly referred to as a "leakage timing circuit."[2] Neither the Final Office Action nor the Answer ever point to any portion of the disclosure in Mizuno et al. that describes OSC20 of Mizuno et al. as "a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current," as claim 1 requires.

Instead, the Answer states, "Mizuno et al.'s figure 12 shows circuit OSC20 (leakage timing circuit), which has a similar structure as circuit OSC1 shown in figure 4, formed on the substrate."[3] However, as noted in the Appeal Brief on page 11, Mizuno et al. in referring to FIG. 3 actually describes OSC1 as "a substrate-bias dependent oscillation circuit," (wherein Mizuno et al. states, "FIG. 4 shows in detail the internal circuit arrangement of each circuit block shown in FIG. 3."[4]) Thus, OSC1 (and thus OSC20 according to the Answer) is described in Mizuno et al. as a "substrate-bias dependent oscillation circuit." However, there is no disclosure in Mizuno et al. with respect to OSC1 in FIG. 3 or FIG. 4 that it is a "leakage timing circuit" as recited in claim 1.

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2 However, Appellants' representatives have performed an electronic search of the Mizuno et al. document, and failed to find the phrase "leakage timing circuit" anywhere in the disclosure of Mizuno et al.
3 *See* the Answer, page 7.
4 *See* Mizuno et al. at column 8, lines 4-11 and column 9, lines 18-19.

In contrast, Mizuno et al. goes on to describe OSC1 in FIG. 4 as actually being a **voltage-controlled oscillator** (VCO). Mizuno et al. states:

> FIGS. 7A and 7B show the relationship of the substrate bias voltage and threshold voltage of the MOS transistors. FIG. 7A is for the NMOS transistors, and FIG. 7B is for the PMOS transistors.
>
> The MOS transistors have their threshold voltage varied depending on the substrate bias as shown in FIGS. 7A and 7B and have a reduced current drive ability for a smaller value of threshold voltage in general, **and accordingly the CMOS ring oscillator OSC1 of FIG. 4 operates as a voltage-controlled oscillator (VCO) in response to the substrate bias signals BP1 and BN1**. On this account, the whole circuit of FIG. 4 has a phase-locked loop (PLL) structure and operates so that the oscillation frequency and phase of the CMOS ring oscillator OSC1 coincide with those of the oscillation output CLK1 of the frequency multiplier PLL1.[5] (Emphasis added).

Thus, Mizuno et al. describes OSC1 of FIG. 4 as being a voltage-controlled oscillator. However, the Final Office Acton and the Answer fail to show that a voltage-controlled oscillator as recited in Mizuno et al. teaches "a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current," as recited in claim 1.

The Final Office Action and the Answer go beyond the prosecution record in an attempt to remedy this deficiency by citing various portions of other documents, such as Miyazaki et al. (U.S. Patent No. 6,489,833) and Teraoka et al. (U.S. Patent No. 6,333,571) in a belated attempt to modify Mizuno et al. to have a circuit that includes a transistor having a backgate bias voltage, and further stating that, ". . . the frequency of the transistor corresponds to its leakage current because they are both related to the backgate bias voltage."[6] However, Appellants submit that the Examiner's logic cites parameters which may be present in a *device,* such as a transistor, and then attempts to project these characteristics of an individual device to be inherent to *a circuit.*

For example, the Answer states, ". . . Miyazaki et al.'s, figure 20 shows the relationship between the threshold of **transistor** and its leakage current."[7] (Emphasis added). The disclosure in Miyazaki et al. with regards to FIG. 20 states,

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5 *See* Mizuno et al. at column 11, line 57 through column 12, line 4.
6 See the Answer, page 7.
7 *See* the Answer, page 7.

> FIG. 20 shows the relation between the threshold of the MOS transistor and the leakage current. In a standard MOS transistor, it is designed with the threshold at point A and the range of variation caused by a process or the like does not exceed the desired limit of a leakage current.[8]

However, a disclosure related to an individual device, such as the transistor of Miyazaki et al., fails to disclose that any circuit that includes a transistor therefore automatically exhibits the trait attributed to the individual transistor. Thus, while the transistor of Miyazaki et al. may include a leakage current, the *circuit* of Mizuno et al. is described as being a voltage-controlled oscillator. The Final Office Action fails to show that a disclosure of a voltage-controlled oscillator, including one or more transistors teaches "**a leakage timing circuit** formed on the substrate, the leakage timing circuit having a frequency related to a leakage current," as recited in claim 1. (Emphasis added).

Independent claims 12, and 16 both include a recitation of a "leakage timing circuit," and claim 26 includes, "generating a second signal related to a leakage current." For reasons analogous to those stated above and in the Appeal Brief on pages 10-12, claims 12, 16, and 26, and claims 2, 6-11, 13-15, 17-18, 27, and 29 which depend from one of claims 12, 16, and 26, are not anticipated by Mizuno et al.

Because claims 1-2, 6-18, 26-27, and 29 are not anticipated by Mizuno et al., there is a clear deficiently in the Final Office Action to set forth a *prima facie* case of anticipation with respect to the rejection of claims 1-2, 6-18, 26-27, and 29. Appellants respectfully request reversal of the rejection and allowance of claims 1-2, 6-18, 26-27, and 29.

The Final Office Action fails to set forth a prima facie case of obviousness in rejecting claims 3-5 and 19-20 in view of the proposed combination of Mizuno et al. and Klemmer because the Final Office Action fails to meet the required burden for setting forth a prima facie case of obvious in the rejection of claims 3-5 and 19-20.

Appellants maintain, as argued on pages 14-18 of the Appeal Brief, that the Final Office Action fails to set forth a *prima facie* case of obviousness in the rejection of claims 3-5 and 19-20 in view of the proposed combination of Mizuno et al. and Klemmer because the Final Office

8 *See* Miyazaki et al. at column 8, lines 6-10.

Action (and now the Answer) have not meet the burden for forming an obviousness rejection with respect to claims 3-5 and 19-20.

As one example of not meeting the burden for forming an obviousness rejection of claims 3-5 and 19-20, the Final Office Action has not shown that the proposed combination of Mizuno et al. and Klemmer teaches or suggests all of the claimed subject matter included in claims 3-5 and 19-20.

Appellants respectfully submit that for at least the reasons stated above with respect to claims 1 and 16, from which claims 3-5 and 19-20 respectively depend, the statements in the Answer fail to remedy the deficiencies in the rejections in the Final Office Action based on the disclosures provided by Mizuno et al. and Klemmer. Neither of these documents provide, either alone or in combination, a teaching or suggestion of the claimed subject matter as included in claims 3-5 and 19-20. Thus, the proposed combination of Mizuno et al. and Klemmer, despite the additional statements made in the Answer, still fails to teach or suggest all of the subject matter as included in each of claims 3-5 and 19-20. The rejection has made no *prima facie* showing of obviousness, and so claims 3-5 and 19-20 are patentable, over the art of record.

Further, and as another example of the Final Office Action failing to meet the required burden in showing *prima facie* obviousness of claims 3-5 and 19-20, Appellants maintain each of the arguments presented on pages 16-17 of the Appeal Brief with respect to the Final Office Action failing to provide a proper basis for forming the proposed combination of Mizuno et al. and Klemmer. In response to those arguments in the Appeal Brief, the Answer merely states, "One skilled in the art would have motivated to add a counter coupled to Mizuno et al.'s OSC10 or OSC20 in order to increasing frequency ratio between the CLK10 and output of OSC10 or OSC20."[9]

Such an argument does not meet the requirements of MPEP § 2143 to show evidence supporting a motivation to combine. The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01.

9 *See* the Answer, page 8

The Answer fails to point to any portion of the disclosure of Mizuno et al. disclosing or suggesting the desirability of increasing the frequency ratio between the CLK10 and the output of OSC10 or OSC20. In fact, as noted on page 16 of the Appeal Brief, Mizuno et al. specifically discloses that the substrate bias voltages BP1 and BN1 are supplied to oscillator circuit OSC1 in order to *lock the frequency* from output S1 of oscillator circuit OSC1 to the frequency of oscillator output CLK1.[10] Thus, the very arguments provided in the Final Office Action and the Answer for forming the proposed combination of Mizuno et al. and Klemmer are contradicted by the disclosure of Mizuno et al. Therefore, statements in the Final Office Action and the Answer fail to meet the requirements of showing the desirability of the combination of Mizuno et al. and Klemmer, and so the Final Office Action and the Answer fail to state a *prima facie* case of obviousness with respect to claims 3-5 and 19-20.

Further, Appellants maintain that the proposed combination of Mizuno et al. with Klemmer would actually destroy the stated purpose of the circuits as described in Mizuno et al. Appellants respectfully submit that the statement in the Answer, "the modified circuit of Mizuno et al. would clearly be operated"[11] is ambiguous, and further, is unsupported by evidence from any cited references in the Answer to the disclosures of either Mizuno et al. and Klemmer. In addition and as noted above, since the disclosure of Mizuno et al. states that voltages are applied to the oscillator circuit OSC1 in order to lock the frequency of the oscillator circuit OSC1 to the CLK1 frequency output, the statements in the Answer regarding the addition of "the counter to the output of Mizuno et al.'s OSC1 if the frequency of CLK1 is lower than desired in order to maintain the desired frequency at the output of OSC1, or if a higher output frequency at OSC1 is needed,"[12] is also unsupported in the Answer by any references to either Mizuno et al. or Klemmer, and would in fact destroy the stated purpose of the circuits of Mizuno et al. as described in Mizuno et al.

Thus, the Final Office Action and the Answer make arguments in support of forming the proposed combination of Mizuno et al. with Klemmer that would destroy the stated purpose of the circuits of Mizuno et al., and so the Final Office Action and the Answer again fail to provide

10 *See* Mizuno et al. at column 8, lines 29-38.
11 *See* the Answer, page 8.
12 *See* the Answer, page 8.

specific, objective evidence of record to support existence of a suggestion or motivation to form the proposed combination. By failing to meet these requirements, the Final Office Action fails to state a *prima facie* case of obviousness with respect to the rejection of claims 3-5 and 19-20.

Because the proposed combination of Mizuno et al. and Klemmer fails to teach or suggest all of the claimed subject matter included in claims 3-5 and 19-20, and because the Final Office Action and the Answer fail to meet the requirements for modifying or combining Mizuno et al. and Klemmer, and further because forming the proposed combination of Mizuno et al. and Klemmer would destroy the stated purpose of Mizuno et al., the Final Office Action and now the Answer have failed to meet the burden of setting forth a *prima facie* case of obviousness with respect to claims 3-5 and 19-20. Appellants respectfully request reversal of the rejection and allowance of claims 3-5 and 19-20.

The Final Office Action fails to set forth a prima facie case of obviousness in rejecting claims 28 and 30 in view of the single reference obviousness rejection based on Mizuno et al. because the Final Office Action fails to meet the required burden for setting forth a prima facie case of obvious in the rejection of claims 28 and 30.

Appellants maintain, as argued on pages 18-19 of the Appeal Brief, that the Final Office Action fails to set forth a *prima facie* case of obviousness in the rejection of claims 28 and 30 in view of the single reference obviousness rejection based on Mizuno et al. because the Final Office Action (and now the Answer) have failed to meet the burden for showing *prima facie* obviousness with respect to claims 28 and 30.

As noted in the Appeal Brief on page 18, the Final Office Action admits that Mizuno et al. fails to show a communication circuit formed on a substrate. The Final Office Action has attempted to use U.S. Patent No 6067612 (hereinafter "Sasaki et al.") and U.S. Patent No. 6044937 (hereinafter "Komori et al.") as disclosing the subject matter of claims 28 and 30 that is missing from Mizuno et al. However, on page 8 of the Answer two new documents, neither of which have been previously cited in the prosecution of the application, are now relied upon. Sasaki et al. and Komori et al. apparently are no longer relied upon. Specifically in the Answer, Kudo (U.S. Patent No. 6,708,289) and Chen (U.S. Patent No. 6,883,078) are now referred to as disclosing that a "microcomputer can be used in cell phone." While Appellants do not necessarily agree or disagree with a statement that a microcomputer can be used in a cell phone,

that hypothetical proposition fails to suggest use of the microcomputer, as described in Mizuno et al., in a communication circuit, since the Examiner admits there is no mention in Mizuno et al. of a "communication circuit."

Further, the statement in the Answer that, "Thus, circuit such as LOG10 is considered a 'communication circuit'"[13] is also unsupported by the disclosure of Mizuno et al. In contrast, Mizuno et al. states, "The main circuit LOG1 is a **CMOS logic circuit** formed of p-channel MOSFETs and n-channel MOSFETs."[14] (Emphasis added). Thus, Mizuno et al. discloses LOG circuits as *logic circuits*, but fails to teach or suggest a *communication circuit*, as implied in the Answer. Without such support in the disclosure of Mizuno et al., the statements in the Answer are an attempted and impermissible reconstruction of the Appellants' claims 28 and 30 using hindsight.

Because the single reference of Mizuno et al. fails to teach or suggest all of the claimed subject matter included in claims 28 and 30, and because the Final Office Action and the Answer fail to provided any other references or evidence suggesting or showing the use of the circuits of Mizuno et al. coupled to a communication circuit, the Final Office Action and the Answer have again failed to meet the Final Office Action's burden of setting forth a *prima facie* case of obviousness with respect to claims 28 and 30. Appellants respectfully request reversal of the rejection and allowance of claims 28 and 30.

13 *See* the Answer, page 8.
14 *See* Mizuno et al. at column 8, lines 15-17.

Conclusion

For at least the reasons argued above, and for at least the reasons presented in the Appeal Brief, claims 1-2, 6-18, 26-27, and 29 were not properly rejected under 35 U.S.C. § 102(b) as being unpatentable over Mizuno et al., claims 3-5 and 19-20 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. in view of Klemmer, and claims 28 and 30 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al.

It is respectfully submitted that the rejections of claims 1-20 and 26-30 based upon the documents cited do not make a *prima facie* showing that claims 1-20 and 26-30 are either anticipated or are obvious. Thus, claims 1-20 and 26-30 are patentable over the cited documents. Reversal of the rejections and allowance of the pending claims is respectfully requested.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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